Stability boundary analysis of the dynamic voltage restorer in weak systems with dynamic loads

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SUMMARY

In this contribution, a stability analysis for a dynamic voltage restorer (DVR) connected to a weak ac system containing a dynamic load is presented using continuation techniques and bifurcation theory. The system dynamics are explored through the continuation of periodic solutions of the associated dynamic equations. The switching process in the DVR converter is taken into account to trace the stability regions through a suitable mathematical representation of the DVR converter. The stability regions in the Thevenin equivalent plane are computed. In addition, the stability regions in the control gains space, as well as the contour lines for different Floquet multipliers, are computed. Besides, the DVR converter model employed in this contribution avoids the necessity of developing very complicated iterative map approaches as in the conventional bifurcation analysis of converters. The continuation method and the DVR model can take into account dynamics and nonlinear loads and any network topology since the analysis is carried out directly from the state space equations. The bifurcation approach is shown to be both computationally efficient and robust, since it eliminates the need for numerically critical and long-lasting transient simulations.

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1. INTRODUCTION

The capacitor-supported dynamic voltage restorer (DVR) is a power electronic converter-based device that has been proposed to protect critical and sensitive loads from supply-side disturbances, except outages [1]. It is connected in series with a distribution feeder and is capable of generating or absorbing reactive power at its ac terminals and interchange real power with the ac network under transient conditions. The operation principle of the DVR is simple; it injects a voltage in series with the feeder. Ideally, this injected voltage is in quadrature with the line current so that the DVR behaves like an inductor or a capacitor for the purpose of increasing or reducing the overall reactive voltage drop across the feeder. In this operating mode, the DVR does not interchange real power with the system in steady-state. The DVR can restore the load-side voltage to the desired amplitude and waveform. The DVR is based on a voltage source converter (VSC). The output of

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the VSC is connected in series with a distribution feeder through a transformer. This device uses IGBTs that are operated in a pulse-width modulated (PWM) fashion. The VSC is supplied by a dc capacitor. A schematic representation of the DVR is shown in Figure 1.

The DVR, including the control system, the compensation algorithm, the loads, and the switching elements, constitutes a nonlinear circuit. In general, a nonlinear circuit can show many interesting phenomena. In this type of circuits, it is frequently found that a steady-state response, such as a limit cycle, abruptly changes its qualitative property by a continuous variation of the system parameters. Such a phenomenon is known as bifurcation of state [2] and is important in the analysis of nonlinear circuits. Upon obtaining the global feature of the bifurcation set, various nonlinear phenomena, such as the coexistence of many stable modes, the jump behavior of periodic responses, the phenomenon of hysteresis and the appearance of chaotic states, etc. can be observed.

In a dynamic nonlinear system, there are mainly two ways to determine the location and stability type of its limit sets. The easiest way to locate a limit set is to integrate the system set of equations until the steady-state is reached. This method is called Brute Force (BF) approach [2]. The commonly adopted technique of BF is frequently limited to the investigation of asymptotically stable steady states. Thus, to explore both stable and unstable periodic orbits, it is necessary to resort to additional properties of differential equations [2].

The BF method has some others serious disadvantages. First, the convergence can take a very long simulation time for poorly damped systems. Second, the BF approach has some drawbacks in locating non-stable and unstable limit sets [2]. On the other hand, a Newton–Raphson (NR) approach is a more efficient way to locate limit sets [2]. This NR method transforms the problem of locating limit sets into a problem of locating the zeros of a dynamical nonlinear system. The main advantages of the NR method are the rapid rate of convergence and the ability to locate non-stable limit sets, as well as unstable and stable limit sets [2].

A suitable framework for the investigation of periodic orbits is the bifurcation theory [2], which in this case is concerned with the structural stability of ordinary differential equations under the variation of one or more system parameters, such as voltages, resistances, inductances, gains of controllers, power demanded, power factor, etc.

Stability analysis based on bifurcation theory of power electronics devices is conventionally carried out using the discrete-time iterative mapping approach [3, 4]. With this approach, the switching converter is essentially modeled as a piecewise switched circuit. The number of possible circuit topologies is usually fixed. This results in a nonlinear time-varying operating mode, which naturally demands the use of nonlinear methods of analysis [3]. In the discrete-time iterative mapping approach, it is usually assumed that the network is linear, and time-invariant between switching instants; thus, the solution between switches can be found in a closed-form [3, 4]. In [5], the dynamical behavior of a full bridge DC–AC buck inverter controlled by fixed frequency and PWM is studied, and an exact solution discrete-time model able to predict both instability
phenomena is derived. In [6], an enhanced modeling method to obtain an accurate description of the converter behavior is presented, and fuzzy techniques are proposed to suppress converter nonlinear phenomena.

For the case of the real power system components based on power electronics technology, it is not easy to represent their mathematical models through a discrete-time iterative mapping approach, since the network between switching instants is nonlinear due to the nonlinear loads connected to the network, the saturated transformers, and other nonlinear network elements.

To understand and control the interactions between the DVR and the power system, there is a need for an appropriate model to obtain both fast and accurate results. However, it is difficult to analyze the dynamics of VSC systems, since they incorporate both continuous time dynamics and switching time events. These analytical difficulties are common in FACTS, Custom Power, and active filters components whose operation is based on power converters. The understanding of the harmonic interaction between the DVR and the network, as well as its impact on the power system stability, can be obtained from an accurate mathematical model of the DVR. This model can give a clear perception about the dynamic performance of the DVR, as well as the possibility to determine the harmonic distortion produced by this device and to assess its adverse impact on power quality and stability, respectively. For this reason, a suitable model for the DVR converter is needed.

Usually, the bifurcation analysis in electric power systems including VSC-based components is carried out using a fundamental frequency converter approximation [7, 8]. This approach is widely used due to its simplicity. However, these models have evident limitations to evaluate the harmonic distortion introduced into the power system by the power converter. In addition, this approximation may not be reliable in the overmodulated region [9]. In addition, there are some other disadvantages with the fundamental frequency models. If the dynamics of the network become close to the switching frequency, this simplification is likely to yield erroneous results, but in some cases the switching frequency significantly differs from the network transient frequencies, thus the simplification would be able to give acceptable results.

Stability analyses in power system are conventionally based on the BF approach and using eigen-analysis [10]. In these analyses, the system is modeled using root mean-square quantities and the electric dynamics are neglected. In this investigation, the power system is represented through instantaneous quantities, the network transients are taken into account and the voltage sources are assumed to be periodic. Besides, the switching process is considered and no simplification or assumption has been considered in order to facilitate the analysis. The continuation techniques are used for the first time in this contribution, to carry out the stability analysis of a power electronic component including the discontinuity and nondifferentiability introduced by the commutating process in the power converter.

2. DVR REFERENCE VOLTAGE GENERATION

The compensation algorithm for the DVR used in this analysis is based on that proposed in [11]. The schematic diagram of a series compensated distribution system is shown in Figure 1. The DVR is connected in series between the point of common coupling (PCC) and the load. The DVR is represented by the voltage sources \( v_{fa}, v_{fb}, \) and \( v_{fc} \); the supply voltages are \( v_{sa}, v_{sb}, \) and \( v_{sc} \); the load voltages are \( v_{la}, v_{lb}, \) and \( v_{lc} \); and the terminal voltages at the PCC bus are represented by \( i_{sa}, i_{sb}, \) and \( i_{sc} \). The critical load is represented by the impedances \( Z_{la}, Z_{lb}, \) and \( Z_{lc} \).

The subscripts \( a, b, \) and \( c \) denote the phases. However, in the following analysis, these are omitted and any equation applies to all three phases. The source is connected to the DVR through a feeder with an impedance of \( R_s + jX_s \). The uppercase characters represent phasor quantities.

With respect to Figure 2, using KVL at PCC bus and neglecting the impedance of the DVR injection transformer, we obtain

\[
V_1 = V_t + V_f
\]
To avoid the interchange of real power in steady-state between the DVR and the network, $V_f$ must be in quadrature with the line current $I_s$. Let us denote the phasor source current as $I_s = |I_s| \angle \theta$, where $|I_s|$ is the magnitude of $I_s$, and $\theta$ is its angle. $I_s$ is obtained from measurements. Therefore, $V_f$ is defined by,

$$V_f = |V_f| \angle \theta + \pi/2$$  \hspace{1cm} (2)

Equation (2) can be represented in rectangular form as:

$$V_f = |V_f|(a_1 + j b_1)$$  \hspace{1cm} (3)

The terminal voltage $V_t$ can be expressed as:

$$V_t = |V_t|(a_1 + j b_1)$$  \hspace{1cm} (4)

From (1), (3) and (4), we obtain,

$$|V_t|^2 + 2|V_t|(a_1 a_1 + b_1 b_1)|V_f| + |V_f|^2 - |V_t|^2 = 0$$  \hspace{1cm} (5)

Equation (5) has two solutions, given by

$$|V_t| = \frac{-b \pm \sqrt{b^2 - 4c}}{2}$$  \hspace{1cm} (6)

where

$$b = 2|V_t|(a_1 a_1 + b_1 b_1)$$  \hspace{1cm} (7)

$$c = |V_t|^2 - |V_f|^2$$  \hspace{1cm} (8)

Negative and complex values of $|V_t|$ are not feasible. The solution that must be chosen from (6) is the real and positive, when a solution exists. If there is not real and positive solution for $|V_t|$, it means that the DVR cannot compensate, no matter what kind of controller is used.

3. DVR STRUCTURE

Figure 3 shows the DVR structure in which a filter capacitor $C_f$ is connected in parallel with the DVR. The instantaneous voltage $v_f$ is the voltage across the filter capacitor $C_f$ [12].

The DVR structure adopted in our analysis is shown in Figure 4. It is a three-leg converter connected to a common dc storage capacitor. The terminals of the VSC are connected to the network through an injection transformer. The inductance $L_T$ represents the transformer leakage inductance and the additional external inductance. The copper loss of the connecting transformer is represented by a resistance $R_T$. The bidirectional switching function is identified by $S_i$ and $S_i'$ for each phase ($i = a, b, c$), which can be on or off, $r$ is the switch-on state resistance, $S_i$ is
1 or 0, corresponding to the on and off states of the switch, respectively. In addition, $S_i$ and $S'_i$ are complementary, e.g. $S_i + S'_i = 1$.

The mathematical model of the three converters shown in Figure 4 is,

$$
L_T \frac{d}{dt} \begin{bmatrix}
i_{Ta}
\i_{Tb}
i_{Tc}
\end{bmatrix} =
\begin{bmatrix}
-(R_T + r)i_a + v_{inj_a} - v_{fa}
-(R_T + r)i_b + v_{inj_b} - v_{fb}
-(R_T + r)i_c + v_{inj_c} - v_{fc}
\end{bmatrix}
$$

(9)

where

$$
v_{inj} = \begin{bmatrix}
S_a - 1/3 \sum_{i=a,b,c} S_i \\
S_b - 1/3 \sum_{i=a,b,c} S_i \\
S_c - 1/3 \sum_{i=a,b,c} S_i 
\end{bmatrix} v_{dc}
$$

(10)

The dynamics of the dc capacitor, $C_{dc}$, is represented by,

$$
\frac{dv_{dc}}{dr} = \frac{1}{C_{dc}} i_{dc}
$$

(11)

where

$$
i_{dc} = -(i_{Ta}S_a + i_{Tb}S_b + i_{Tc}S_c)
$$

(12)

$v_{inj}$ is the voltage at the converter terminals. This voltage is represented in terms of the switching functions $S_a$, $S_b$, and $S_c$, which is advantageous since the model will not be dependent on the selected PWM technique.

According to (10), (11) and (12), the DVR model is a discontinuous time-varying system since the switching function $S_i$ instantaneously changes from one state to another. Under these conditions, the conventional numerical integration does not give numerical solutions to a high precision.
In addition, the stability analysis through the bifurcation theory using continuation techniques cannot be efficiently used. In fact, the discontinuity in power electronic converters is the principal obstacle for using the continuation techniques in the stability analysis based on the bifurcation theory. For example, in FACTS devices, fundamental frequency model is frequently used due to its simplicity. Conventionally, when the switching process is taken into account, the bifurcation diagrams are computed through the BF approach [3, 4].

To avoid these drawbacks, the two models for the representation of the VSC proposed in [13] can be used to perform the bifurcation analysis. In particular for this investigation, the hyperbolic tangent model [13] is used; however, the Fourier series approach model can also be used.

4. CLOSED-LOOP COMPENSATION SCHEME

The compensation algorithm represented by (6) gives the magnitude of the voltage that must be injected in series by an ideal DVR (no voltage drop across the injection transformer) to compensate the magnitude of the voltage at the load bus. We can see (6) as an open-loop compensation algorithm. However, for a real case, there is a voltage drop across the injection transformer. Therefore, an open-loop compensation scheme is not suitable to compute the voltage that must be injected by the DVR, and a feedback compensation algorithm is needed instead. For this case, a simple PI-controller is used; this is given by

\[
|V_{\text{ref}}| = K_{vp}(|V_{\text{ref}}^-| - |V_i|) + K_{vi} \int (|V_{\text{ref}}^-| - |V_i|) \, dt
\]  

(13)

where \( |V_{\text{ref}}^-| \) is the load voltage reference magnitude, \( |V_i| \) is the load voltage magnitude, obtained from measurements. Thus, the closed-loop compensation algorithm is given by:

\[
|V_{\text{inj}}|^2 + 2|V_i|(|a_1 a_1 + b_1 b_1|V_{\text{inj}}| + |V_i|^2 - |V_{\text{ref}}|^2 = 0
\]  

(14)

A feasible solution of (14) is

\[
|V_{\text{inj}}| = \min \left( \frac{-b \pm \sqrt{b^2 - 4c}}{2} \right)
\]  

(15)

where

\[
b = 2|V_i|(|a_1 a_1 + b_1 b_1| \quad (16)
\]

\[
c = |V_i|^2 - |V_{\text{ref}}|^2
\]  

(17)

Figure 5 illustrates the DVR control system, where \( m \) is the amplitude modulation ratio and \( \alpha \) is the phase of the voltage control signal at the converter terminal.
The performance of the DVR directly depends on its control system; however, there are some limitations that are not associated with the control systems but with the compensation limits of the DVR. These compensation limits are given by the solutions of (14); if there is not a real and positive solution, it means that the DVR is beyond its compensation limits, which imply that no matter what compensation algorithm, control scheme, or gains set are used, the DVR will not properly compensate. For more details about the feasible solutions of the DVR, please see [11].

5. CONTINUATION TECHNIQUES

The continuation techniques are employed to compute the solution manifolds of nonlinear systems. In general, the power system and the power electronics components are represented by a set of nonlinear differential equations, nonlinear difference equations, and nonlinear algebraic equations. For instance, for the case of the DVR, the nonlinear differential equations are associated with the network variables and the load, the nonlinear difference equations are associated with the digital implementation of the control scheme, and the nonlinear algebraic equations are associated with the computation of the switching functions.

The bifurcation theory can be applied to different control schemes; e.g. it is used in [14] to assess the stability boundaries of DSTATCOM operating as voltage regulator with a dead-beat (discrete-time) control [15] considering a dynamic and nonlinear load in a non-stiff system. A similar analysis is carried out in [16] using a control based on the instantaneous symmetrical components theory. There are no limitations for the application of this theory to any other control method or power converter [17].

In this contribution, the sequential method [18] is used as the predictor and the Newton method based on the discrete exponential expansion method [19] is used as the corrector.

In the sections to follow, bifurcation theory will be applied to compute the stability regions of the electric system including the DVR shown in Figure 1. The detailed DVR model based on the hyperbolic tangent [13] is used to construct the bifurcations diagrams; however, the model based on the Fourier approach [13] can be also used.

6. DVR BIFURCATION ANALYSIS

In this section, the bifurcation theory is applied to the electric system shown in Figure 1 to assess its stability regions. For this particular case, the control system used for the DVR is that of Figure 5; however, another control system can be used. In the following section, bifurcation diagrams in the Thevenin space are computed to show the set of $X_s$, $R_s$, and $v_s$ for which the DVR contains stable solutions. The stability regions in the gains space are calculated through bifurcation theory, and the set of gains for the fastest speed response of the DVR is obtained from this analysis. Besides, the gains impact on the stability in the Thevenin space is analyzed. Finally, the ac and dc capacitors impact on the stability in the Thevenin space is analyzed.

The fundamental frequency models of the VSCs have been widely used for the analysis and application design of power electronic devices in electric power systems. This is basically due to its simplicity in comparison with more detailed models where the switching process is taken into account. It is clear that the detailed models retain more nonlinearities (more information) than the fundamental frequency models and consequently represent better the behavior of a real system; however, they are complex since they incorporate continuous and discrete variables. In practice, we should only use a fundamental frequency model for analysis or characterization of phenomena which occur as fast as an order of magnitude below the switching frequency. Clearly, the fundamental frequency models disregard all high-frequency details, and hence are not suitable for characterizing high-frequency or fast-scale dynamics.

In a practical case, we prefer the fundamental frequency models over the detailed models where the switching process is taken into account since the formers are simpler than the last ones; however, we cannot know if the fundamental frequency model will give proper results until we
Figure 6. Stability regions for the DVR in the $X_s-R_s$ plane for different Thevenin equivalent voltages using the fundamental frequency model.

6.1. Stability regions in the $X_s-R_s$ plane

The network of Figure 1 has been represented through its Thevenin equivalent. The network upstream from the PCC towards the source side may contain different feeders and loads. Thus, the radial line and the source shown in Figure 1 are a Thevenin representation of the upstream network, where $v_s$, $R_s$, and $X_s$ represent the Thevenin equivalent looking towards the left into the network.

Since the Thevenin equivalent can change any time dependence on the load at the left side of PCC, it is desirable to assess a set of $v_s$, $R_s$, and $X_s$, for which the DVR performance is stable.

6.1.1. Comparison between the fundamental frequency model and the detailed model with low-frequency modulation ratio.

The Figure 6 shows the bifurcation set on the $X_s-R_s$ plane computed using the fundamental frequency model of the DVR converter. This figure shows the stability regions for different Thevenin equivalent voltages, i.e. for $|V_s| = 0.9 \text{ pu}$ in Figure 6(a), for $|V_s| = 1 \text{ pu}$ in Figure 6(b), and for $|V_s| = 1.1 \text{ pu}$ in Figure 6(c), where $|V_s|$ is the peak value of $v_s$. The rest of the parameters are those given in Appendix A. The solid line represents the Neimark–Sacker (NS) [2, 18] bifurcation set. This bifurcation corresponds to a quasiperiodic solution. Inside the contour line, the solutions are $T$-periodic. For the electric system shown in Figure 1, only the NS bifurcation was located in the parametrical-space using the fundamental frequency model of the DVR converter. Observe that the magnitude of the voltage source has a positive impact on the size of stability regions in the $X_s-R_s$ plane.

To corroborate the bifurcation diagrams shown in Figure 6, these are computed again using now the detailed model, which includes the harmonic distortion produced by the converter-switching process. The purpose of this simulation experiment is to assess the harmonic interaction between the...
DVR and the power network. Figure 7 shows the bifurcation diagram computed using the detailed model of the DVR converter. For this analysis, the frequency modulation ratio used is $m_f = 9$ (540 Hz), and the highest harmonic order included in this analysis is 113 (6780 Hz). Comparing Figures 6 and 7, we can observe that the solutions given by the fundamental frequency model and the detailed model are noticeably different. In addition, the detailed model predicts the supercritical symmetry-breaking bifurcation (Sup. SB), and the NS [18]. In the Sup. SB bifurcation, the stable branch of symmetric periodic solutions, which exist prior to the bifurcation, continues as an unstable branch of symmetric periodic solutions after the bifurcation. In addition, two locally stable asymmetric periodic solutions coexist with unstable symmetric periodic solutions. The maximum and minimum of an asymmetric periodic solution differ.

Figure 8 shows the bifurcation diagram for $|V_s| = 1\text{pu}$, $X_s = 1.31\text{pu}$, with $R_s$ taken as the bifurcation parameter. Please notice that close to $R_s = 0.405\text{pu}$ a Sup. SB bifurcation occurs. In addition, a NS bifurcation is born at $R_s = 0.325\text{pu}$ and disappears at $R_s = 0.38\text{pu}$. At $R_s = 0.45\text{pu}$, a NS bifurcation is born in the two locally stable asymmetric periodic solutions.

Figure 9 shows the quasiperiodic solution in $i_{sa} - v_{fa}$ plane, with $R_s = 0.22\text{pu}$, $X_s = 1.13\text{pu}$ and $|V_s| = 1\text{pu}$. This operating point corresponds to a quasiperiodic solution. This solution agrees with the bifurcation analyses which predict quasiperiodic solutions for this operating point.

6.1.2. Comparison between the fundamental frequency model and the detailed model with higher-frequency modulation ratio. Figure 10 illustrates the bifurcation set in the $X_s - R_s$ plane computed using the detailed model of the DVR converter. This figure shows the stability regions for different Thevenin equivalent voltages, e.g. $|V_s| = 0.9\text{pu}$ in Figure 10(a), $|V_s| = 1\text{pu}$ in Figure 10(b), and $|V_s| = 1.1\text{pu}$ in Figure 10(c). For this analysis, the frequency modulation ratio is $m_f = 27$ (1620 Hz), and the highest harmonic order included in the analysis is 113. Please notice that the bifurcation diagrams in Figure 10 are identical to those given in Figure 6.

From the conducted experiment, it can be observed that the harmonic distortion has an important effect on the stability of the DVR, thus the harmonic distortion cannot be neglected. Under these conditions, the fundamental frequency model would give erroneous results because the harmonic interaction between the DVR and the electric system is neglected; however, for cases where
the switching frequency significantly exceeds the network transient frequencies, the fundamental frequency model would give reliable results. Hereafter, the frequency modulation ratio used will be $m_f = 27$, and the highest harmonic order included in this analysis will be 113 [13].

6.2. Stability regions in the gains plane

The stability region in the gains space is useful for some practical applications: first, it determines the whole set of gains for which the system stability is preserved, and second, because it is easy to know the speed of response directly from the Floquet multipliers.

In this section, the stability region in the $K_{qp} - K_{qi}$ space, and in the $K_{vp} - K_{vi}$ space is computed, as well as the contour lines for different Floquet multipliers.

Figure 11 shows the stability regions in the $K_{qp} - K_{qi}$ space. In this figure, contour lines are presented for different Floquet multipliers to show the different speed of response. From this figure it can be noticed that there is a large area in the plane $K_{qp} - K_{qi}$ for which the speed of response is very similar, so we can select any set of gains $K_{qp} - K_{qi}$ in this area. However, for practical applications, a large set of gains is not a good choice. A smaller set of gains has an easier implementation, e.g. $K_{qp} = 0.6$ and $K_{qi} = 180$.

Now, the stability region in the $K_{vp} - K_{vi}$ plane is shown in Figure 12 for the set of gains $K_{qp} = 0.6$ and $K_{qi} = 180$ chosen from Figure 11. The set of gains for the load voltage controller is selected from Figure 12 as $K_{vp} = 0.2$, and $K_{vi} = 100$. Thus, the whole set of gains are now selected as $K_{qp} = 0.6$, $K_{qi} = 180$, $K_{vp} = 0.2$, and $K_{vi} = 100$.

To show the impact of the selected set of gains on the DVR stability, the stability regions in the Thevenin equivalent space are shown in Figure 13, i.e. for $V_s = 0.9$ pu in Figure 13(a), $V_s = 1$ pu.
Figure 10. Stability regions for the DVR in the $X_s-R_s$ plane for different Thevenin equivalent voltages using the detailed model.

Figure 11. Stability regions for the DVR in the $K_{op}$-$K_{oi}$ space.

in Figure 13(b), and $|V_s|=1.1$ pu in Figure 13(c), respectively. Notice that the stability boundaries have been increased, as compared with those shown in Figure 10. The set of gains I is given in Appendix A, and the set of gains II is $K_{op}=0.6$, $K_{oi}=180$, $K_{vp}=0.2$, and $K_{vi}=100$.

The selected set of gains obtained with the bifurcation analysis improves the stability region and the speed of response of the DVR.

6.3. AC Capacitor impact on the stability

The main purpose of the ac capacitor filter is to reduce the harmonic content of the injected voltage by the converter. For a low value of $X_f$, the capacitor current is high, while this current reduces
with the increase in the value of $X_f$. In effect, a reduction of $X_f$ behaves like a short circuit, and the DVR cannot properly compensate, while a large value of $X_f$ makes the filtering inadequate [12]. The value of the ac capacitor filter influences the filtering performance; besides, this impacts the stability of the DVR. To assess the ac capacitor filter impact on stability, the stable regions in the Thevenin plane have been compared for three different ac capacitors; this comparison can be seen in Figure 14. From this figure, it is easy to notice that the ac capacitor size has a negative impact on stability, since the stable region on the $X_s$–$R_s$ plane reduces as the capacity of the ac capacitor increases.

From the results shown in Figure 14, it is possible to observe that for a good selection of $C_f$, two important design specifications have to be taken into account: (1) the THD in load voltage
should be within a limit of 5% [20], and (2) that the stability region should be the maximum possible, since it means that inside of this region the DVR can properly compensate the load voltage. Therefore, we can deduce that the optimum value of $C_f$ is that for which the maximum THD inside of the stable region is 5%. It is important to notice, for this particular case, that if the maximum THD is reduced by increasing $C_f$, then the stable region in the $X_s - R_s$ plane becomes smaller, which is undesirable for practical purposes.

Figure 15 shows the stability region in the $X_s - R_s$ plane for $X_f = 21$ pu. In addition, the THD in the load voltage is plotted in this figure as contour lines; it is observed that the THD is within the limits inside the stable region in the $X_s - R_s$ plane. Thus, from the simulation experiment the ac capacitor is selected as $X_f = 21$ pu.
6.4. dc Capacitor impact on the stability

The dc capacitor is a very important element in the design of the DVR, as it stores the necessary energy to compensate the load during disturbances. In steady state, the DVR has to provide the active power fluctuation and the reactive power demanded by the system, in order to maintain the voltage at the PCC bus. Thus, the dc capacitor size is important for the compensator performance; i.e. for large capacitances, the stored energy is high; consequently, the DVR can bear larger and more severe disturbances. This observation suggests that the stable region increases as the dc capacitor size becomes larger. Figure 16 shows the stability region in the $X_{dc} - |V_s|$ plane. It can be seen from Figure 16 that the capability to compensate voltage sags by the DVR increases as the dc capacitor becomes larger. From this analysis, the dc capacitor size can be selected to suit the load demand, e.g. $X_{dc} = 9.2\, \text{pu}$ for this case. It can be seen that the largest size of the dc capacitor is not the best choice. For example, from Figure 16, it is easy to observe that for reactances below $X_{dc} = 9.2$ the maximum sag that can be compensated by the DVR does not significantly change, in fact, the maximum sag that can be compensated by the DVR decreases as the $X_{dc}$ becomes smaller than 9.2 pu, therefore, the dc capacitor size has to be selected using the maximum voltage ripple as an auxiliary criterion for design. In Figure 16 contour lines showing the maximum voltage ripple in the dc capacitor are in addition plotted.

It is observed from Figure 16 that the maximum voltage ripple in the dc capacitor for $X_{dc} = 9.2\, \text{pu}$ is 5% [9], which remains within limits. To corroborate the bifurcation diagram shown in Figure 16, various time domain simulations were carried out for different Thevenin voltages. Initially, the system including the DVR is in periodic steady state with $|V_s| = 1\, \text{pu}$. Then at $t = 0.1\, \text{s}$ the Thevenin voltage magnitude is changed from $|V_s| = 1\, \text{pu}$ to $|V_s| = 0.92\, \text{pu}$; for this operating point, the DVR properly compensates, as we expected from Figure 16. However, when $|V_s|$ is decreased to $|V_s| = 0.82\, \text{pu}$ for $t \in [0.3, 2.5] \, \text{s}$, the power system becomes unstable and a chaotic solution appears. At $t = 2.5\, \text{s}$ $|V_s|$ is increased to $|V_s| = 0.86\, \text{pu}$; for this operating point the DVR correctly compensates. All these changes in the Thevenin voltage are shown in the waveforms of Figure 17. The dc capacitor voltage $v_{dc}$, and the mean magnitude of the load voltage $|V_l|$ are shown in Figure 17(a) and (b), respectively. These observations agree with the bifurcation diagrams shown in Figure 16. In addition, observe that the maximum voltage ripple at the dc capacitor does not exceed 5% in the stable operation of the DVR. Thus, for the conducted experiment the dc capacitor is selected as $X_{dc} = 9.2\, \text{pu}$ (gray lines).

Figure 18 shows how the quasiperiodic solution in the $i_{sa} - v_{f0}$ plane becomes chaotic when $|V_s|$ is changed from 0.82 to 0.81 pu. In Figure 18(a) the solution in the $i_{sa} - v_{f0}$ for $|V_s| = 0.82\, \text{pu}$; this form describes a quasiperiodic solution. On the other hand, in Figure 18(b) the solution in the
7. FEASIBLE SOLUTIONS OF THE DVR

The real and positive solutions of (14) are the feasible solutions of the DVR. In particular, for the test systems shown in Figure 1, the feasible solution in the $X_s - R_s$ plane is limited by $R_s$; e.g. for $|V_s| = 1$ pu, $|V_f| = 1$ pu, $Z_f = 2 + j1.8$ pu, the feasible solution in the $X_s - R_s$ plane is limited by $0 \leq X_s \leq \infty$, and $0 \leq R_s \leq 0.69$ pu. Most of these solutions are impractical, since large values of $|V_f|$ are necessary for large values of $X_s$. In addition, very large values of $X_s$ are not present in a real feeder or transmission line.
In a more realistic case, the power converter capability imposes additional restrictions to the feasible solutions of the DVR. Such restrictions are basically associated with the injected voltage saturation when the converter is operating in the nonlinear region, e.g. $m > 1$. In the nonlinear region, the harmonic distortion increases in the voltages injected by the converter, which is undesirable. In this investigation, the converter has been only operated in the linear region.

Figure 19 shows a comparison between the feasible solution and the stability region in the $X_s$–$R_s$ plane for $|V_s| = 0.9\, \text{pu}$, $|V_s| = 1\, \text{pu}$, and $|V_s| = 1.1\, \text{pu}$ in Figures 19(a), (b), and (c), respectively. In these Figures, the amplitude modulation index has also been included. An amplitude modulation index of 0.9 has been imposed to the feasible solution; however, the power converter can be operated in the nonlinear region, e.g. $m > 1$.

It can be noticed that the feasible solution, even for an amplitude modulation index of 0.9 is larger than the stability region. However, it has been shown in Figures 16 and 15 that the stability boundary can be increased if the dc capacitor size is increased and/or the ac filter capacitor size is decreased, respectively. To increase the dc capacitor size increase its price, and to decrease the ac filter capacitor size increase the THD in the load voltage. For these reasons they could not be practical options to increase the stability region.

In order to illustrate some possible options to increase the stable boundary of the DVR, a comparison between the stability regions in the $X_s$–$R_s$ plane for different options of ac and dc capacitor sizes are shown in Figure 20. The shadow region shows the feasible solution in the $X_s$–$R_s$ plane for different amplitude modulation indexes. In addition, the stability boundary for different sets of dc and ac capacitor is presented. The contour line A will be taken as the base
8. CONCLUSION

A stability analysis of the DVR based on bifurcation theory using a detailed model of the DVR has been presented. The detailed model used in this analysis includes the switching process in the DVR converter. The bifurcation analysis has been performed using continuation techniques and a Newton method based on a discrete exponential expansion matrix and extrapolation to the limit cycle procedure.

It has been shown that by moving the system parameters smoothly, the system exhibits loss of stability; an NS bifurcation appears when the fundamental frequency model is used. On the other hand, an NS bifurcation and supercritical breaking symmetry bifurcation appear when the detailed model of the DVR is used.

It has been shown, through bifurcation analysis, that the widely used fundamental frequency model yields erroneous results if the switching frequency is close to the network transient frequency; the results given by the fundamental frequency model would be reliable if the switching frequency is far from the network transient frequencies.

Bifurcation diagrams in the $X_s$–$R_s$ plane for different Thevenin voltages have been presented. In addition, the bifurcation diagrams in the $K_{op} - K_{oi}$ space and in the $K_{oi} - K_{vp}$ space have been presented. From these bifurcations diagrams in the gains space, the set of gains for the DVR has been obtained.
The effect on the DVR performance and the stability of the dc storage capacitor, as well as the AC filter capacitor, has been shown. For the case of the dc storage capacitor, it has been demonstrated that the capacitor size has a positive effect on the DVR stability. On the other hand, the AC filter capacitor size has an adverse impact on the DVR stability. In addition, the AC capacitor filter and the dc storage capacitor have been designed using the bifurcation theory.

It has been demonstrated that the bifurcation theory can be successfully applied to assess nonlinear oscillations in distribution systems containing DVR. An assessment of qualitative effects of electrical parameters on the stability and on the speed of response of the DVR has been detailed. This analysis allows an effective selection of the DVR parameters to ensure the rated operation condition of the DVR far away from a possible bifurcation. In addition, the bifurcation analysis allowed increasing the stability boundary up to the boundary of feasible solutions.

APPENDIX A

The electric and control parameters of the case study shown in Figure 1 are given in Table AI.

Table AI. Systems parameters.

<table>
<thead>
<tr>
<th>Systems parameters</th>
<th>DVR</th>
</tr>
</thead>
<tbody>
<tr>
<td>System voltage ($</td>
<td>V_s</td>
</tr>
<tr>
<td>Feeder impedance ($R_s$, $X_s$): 0.05 + j0.94 pu</td>
<td>$V_1$ control loop gains: $K_{dip}=0.05$, $K_{dzi}=180$.</td>
</tr>
<tr>
<td>AC capacitor ($X_{ac}$): 17.6 pu</td>
<td>dc capacitor ($X_{dc}$): 8.84 pu</td>
</tr>
<tr>
<td>Load impedance ($R_l$, $L_l$): 2 + j1.8 pu</td>
<td>Injection transformer impedance ($R_T$, $L_T$): 0.02 + j0.19 pu</td>
</tr>
</tbody>
</table>

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